

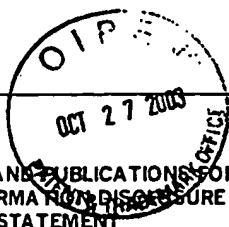
PATENT APPLICATION

Sheet 1 of 3

FORM PTO-1449

LIST OF PATENTS AND PUBLICATIONS FOR
APPLICANT'S INFORMATION DISCLOSURE
STATEMENT

(Use several sheets if necessary)



ATTY. DOCKET NO.

200309657-1

APPLICATION NO.

10/652,847

CONFIRMATION NO.

APPLICANT

Peter M. Martino

FILING DATE

08/29/2003

GROUP

REFERENCE DESIGNATION

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	PUBLICATION DATE	NAME	Pages, Columns, Lines Where Relevant Passages or Figures Appear
YS	1A	6,596,561	7/22/2003	Takahashi et al.	
YS	1B	6,583,040	6/24/2003	Lin	
YS	1C	6,531,947	3/11/2003	Weaver et al.	
YS	1D	6,529,023	3/4/2003	Becker et al.	
YS	1E	6,528,892	3/4/2003	Caketka et al.	
YS	1F	6,490,161	12/3/2002	Johnson	
YS	1G	6,477,058	11/5/2002	Luebs et al.	
YS	1H	6,384,487	5/7/2002	Smith	
YS	1I	6,333,460	12/25/2001	Toy et al.	
YS	1J	6,320,267	11/20/2001	Yukawa	
YS	1K	6,312,791	11/6/2001	Fasano et al.	

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	PUBLICATION DATE	NAME OF PATENTEE OR APPLICANT	Pages/Columns/Lines Where Relevant Passages/Figures Appear	Check if Translation attached
	1L					
	1M					
	1N					
	1O					
	1P					

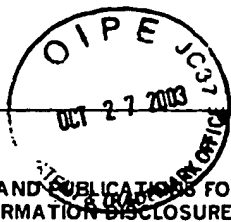
OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, etc.)

YS	1Q	Greenzweig, Yuval, "Micro-Surgery of C4 Microprocessors and Future Developments," Intel Corporation, MTM, Haifa, Israel (2 pages).
YS	1R	IBM Corporation, "Flip-chip packaging services," Hopewell Junction, New York, April 2003 (4 pages).
YS	1S	IBM Corporation, "Multilayer ceramic (MLC) packaging," Hopewell Junction, New York, April 2003 (4 pages).

EXAMINER

DATE CONSIDERED

12/01/2005



PATENT APPLICATION

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YS	2A	6,222,263	4/24/2001	Sherif et al.	
YS	2B	6,191,480	2/20/2001	Kastberg et al.	
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YS	2D	5,677,247	10/14/1997	Hundt et al.	
YS	2E	5,650,593	7/22/1997	McMillan et al.	
YS	2F	5,413,489	5/9/1995	Switky	
	2G				
	2H				
	2I				
	2J				
	2K				

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	2N					
	2O					
	2P					

OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, etc.)

YS	2Q	Intel, "Chip Scale Pack for Intel Flash Memory Devices - Packaging Overview," http://www.intel.com/design/flcomp/PRODBREF/298113.htm (visited August 13, 2003) (4 pages).
YS	2R	Intel, "Semiconductor Technology and Manufacturing," http://www.intel.com/technology/itj/2002/volume06issue02/art07_emergingdirections/p06... (visited August 13, 2003) (3 pages).
YS	2S	Mahajan, Ravi, Raj Nair, Vijay Wakharkar, Johanna Swan, John Tang, Gilroy Vandentop, "Emerging Directions for Packaging Technologies," Intel Technology Journal, Vol. 6, Issue 02, May 16, 2002 (pages 62-75).

EXAMINER

Yuriy Serebrennikov

DATE CONSIDERED

12/01/05

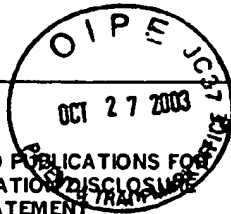
PATENT APPLICATION

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FORM PTO-1449

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	3A				
	3B				
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	3D				
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	3L					
	3M					
	3N					
	3O					
	3P					

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YS	3Q	* Packaging Information - Package Reference Guide," http://www.icw.ave.com/technical/docs/package/guide.htm (visited August 13, 2003) (4 pages).
YS	3R	Tyco Electronics, "Metallized Particle Interconnect Applications Guide," North Attleboro, Massachusetts (pages 1-9).
YS	3S	Vicich, Brian and Sai Uppuluri, "Nonlinear Analysis Helps Design LGA Connectors," http://connectorspecifier.printthis.clickability.com/pt/cpt?action=cpt&expire=&urlID=408... (visited August 13, 2003) (4 pages).

EXAMINER

Yuriy Seleznev

DATE CONSIDERED

12/01/2005